REMARKS

Claims 2-6 and 21-34 are all the claims pending in the application, where claims 2-6 and 21-34 are amended, and claim 1 is canceled. These are merely a clarifying amendments, and are not believed to affect the scope of the claims in any way, and no estoppel is intended.

Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 2, 4-6 and 21-34 are allowed.

Claim Rejections under 35 U.S.C. § 112

Claim 1 is rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Claim 1 is canceled, thereby rendering the Examiner's rejection moot.

Claim Rejections under 35 U.S.C. § 102

Claim 3 is rejected under 35 U.S.C. § 102(b) as being anticipated by Luo (U.S. Patent No. 6,48 6,739). For at least the following reasons, Applicant traverses the rejection.

The Examiner relies on FIG. 1 of Luo as allegedly corresponding to the claimed invention. The circuit shown in FIG. 1 of Luo merely corresponds to the input stage of the claimed circuit, in which a capacitance is formed between an input terminal and a bias line, and in which a resistance which is inserted in series with the bias line is connected to the input terminal via the capacity, as shown in FIG. 40 of the instant specification.

In contrast, claim 3 corresponds to the circuits as shown in FIG. 24 or FIG. 25 of the instant specification. In the circuit as shown in FIG. 24, impedance element 2 is connected to the input terminal. In the circuit as shown in FIG. 25, an impedance element, comprising of resistors

13 and 30 and capacitor 14, is connected to the input terminal. The construction in which an impedance element is connected to the input terminal is a feature recited in claim 3. For example, claim 3 recite "a first impedance element **which does not block a direct current**". That is, in the amplifier according to claim 3, when an input signal is supplied to the following amplifier stage (Tr1) via the impedance element, direct current is not blocked.

In contrast, the circuit of Lao relied upon does not have the above construction. In Lao an input signal is supplied to the following amplifier stage Q1 via a capacitor C1 (Lao: FIG. 1). The capacitor C1 would have an infinite impedance when direct current is input and would therefore **block** direct current. Additionally, the circuit has the following defects:

(a) when the value of the resistor R1 is small, the circuit exhibits a gain extension characteristic, but the phase of inter-modulation distortion (IM3) does not rotate;

(b) when the value of the resistor R1 is large, the phase of inter-modulation distortion (IM3) rotates, but the circuit does not exhibit a gain extension characteristic.

Accordingly, Applicant respectfully submits that claim 3 is patentable over the applied reference.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

/ Rohit K. Krishna /

Rohit K. Krishna
Registration No. 62,474

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: September 30, 2008